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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,054	11/14/2003	Kiyoshi Hasegawa	OKI.118D2	9019

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/712,054	HASEGAWA ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19,20,23,24,27-31 and 34-36* is/are rejected.

7)☒ Claim(s) *21,22,25,26,32 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 1-18 have been withdrawn and cancelled from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/29/04.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 19, 20, 23, 24, 27-31, & 34-36 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,207,477 Motooka et al.

2. Referring to claim 19, a semiconductor intermediate product, comprising: a semiconductor wafer, (Figure 4 #2A), having a plurality of device surface areas, (Figure 4 area of #3A), which are separated from one another by scribe lines, (Figure 4 #2B), wherein each of the device surface areas, (Figure 4 area of #3A), includes a substrate mounting region, (Figure 4 area of #3A), and a plurality of surface electrodes, (Figure 4 #8A), adjacent the substrate mounting region, (Figure 4 area of #3A); a plurality of wiring substrates, (Figure 4 #6), fixed to the substrate mounting region of the plurality of device surface areas, (Figure 4 area of #3A),

respectively, wherein a peripheral surface region of each of the wiring substrates, (Figure 4 #6), includes a plurality of electrode pads, (Figure 4 #8b); a plurality of wiring bondings, (Figure 4 #4), which connect the plurality of electrode pads, (Figure 4 #8b), to the plurality of surface electrodes, (Figure 4 #8A), within each of the plurality of device surface areas, (Figure 4 area of #3A); and a resin, (Figure 4 #1), contained between adjacent wiring substrates, (Figure 4 #6), so as to cover the scribe lines, (Figure 4 #2B), the electrode pads, (Figure 4 #8B), the wiring bonding, (Figure 4 #4), and the surface electrodes, (Figure 4 #8A), between the adjacent wiring substrates, (Figure 4 #6), within the resin, (Figure 4 #1).

3. Referring to claim 20, a semiconductor intermediate product, further comprising an insulating adhesive, (Figure 4 #3A), which fixes wherein the plurality of wiring substrates to the substrate mounting region of the respective plurality of device surface areas.

4. Referring to claim 23, a semiconductor wafer product comprising: a semiconductor wafer, (Figure 4 #2A), having a plurality of chip areas, (Figure 4 area of #3A), and a plurality of scribe areas, (Figure 4 #2B), that divide the chip areas, (Figure 4 area of #3A), each of the chip areas, (Figure 4 area of #3A), having a central area at which an integrated circuit is formed and an electrode area, (Figure 4 area of #8A), surrounding the central area, wherein a plurality of first electrode pads, (Figure 4 #8A), are formed in the electrode area, (Figure 4 area of #8A); a plurality of wiring substrates, (Figure 4 #6), formed on the central areas, each of the wiring substrates, (Figure 4 #6), having a plurality of external electrodes, (Figure 4 #8C & 7), formed in a center area thereof and a plurality of second electrodes pads, (Figure 4 #8B), respectively electrically connected to the external electrodes, (Figure 4 #7 & 8C), formed in a peripheral area thereof, a plurality of bonding wires, (Figure 4 #4), each of which respectively connects one of

the first electrode pads, (Figure 4 #8A), with one of the second electrode pads, (Figure 4 #8B); and a resin, (Figure 4 #1), formed on the electrode areas, (Figure 4 #8A&B), the peripheral areas of the wiring substrates, (Figure 4 #6), and the scribe areas, (Figure 4 #2B), so that the resin, (Figure 4 #1), covers the first and second electrode pads, (Figure 4 #8A&B), and the bonding wires, (Figure 4 #4).

5. Referring to claim 24, a semiconductor wafer product, wherein a plurality of scribe lines are formed on the scribe areas, (Figure 4 #2B).

6. Referring to claim 27, a semiconductor wafer product, wherein a top surface of the resin, (Figure 4 #1), has substantially the same level as top surfaces of the wiring substrates, (Figure 4 #6).

7. Referring to claim 28, a semiconductor wafer product, wherein the external electrodes, (Figure 4 #7 & 8C), are formed in peripheral regions of the central areas of the wiring substrates, (Figure 4 #6).

8. Referring to claim 29, a semiconductor wafer product, wherein the external electrodes are ball electrodes, (Figure 4 #7).

9. Referring to claim 30, a semiconductor wafer product comprising: a semiconductor wafer, (Figure 4 #2A), having a plurality of chip regions, (Figure 4 area of #3A), and scribe regions, (Figure 4 #2B), separating the chip regions, (Figure 4 area of #3A), wherein each of the chip regions, (Figure 4 area of #3A), has a central region at which an integrated circuit is formed and a peripheral region at which a plurality of first electrode pads, (Figure 4 #8A), are formed; a plurality of wiring substrates, (Figure 4 #6), respectively formed on the central regions of the chip regions, (Figure 4 area of #3A), wherein each of the wiring substrates, (Figure 4 #6), has a

plurality of external electrodes, (Figure 4 #7 & 8C), formed in a center area thereof and a plurality of second electrode pads, (Figure 4 #8B), respectively electrically connected to the external electrodes, (Figure 4 #7 & 8C), formed in a peripheral area thereof, a plurality of bonding wires, (Figure 4 #4), respectively connecting the first electrode pads, (Figure 4 #8A), with the second electrode pads, (Figure 4 #8B); and a resin material, (Figure 4 #1), formed on the semiconductor wafer, (Figure 4 #2A), except for the center areas of the wiring substrates, (Figure 4 #6), so that the resin material, (Figure 4 #6), covers the first, (Figure 4 #8A), and second electrode pads, (Figure 4 #8B), and the bonding wires, (Figure 4 #4).

10. Referring to claim 31, a semiconductor wafer product, wherein a plurality of scribe lines are formed in the scribe regions, (Figure 4 #2B), of the semiconductor wafer, (Figure 4 #2A).

11. Referring to claim 34, a semiconductor wafer product, wherein a top surface of the resin, (Figure 4 #1) material has substantially a same level as top surfaces of the wiring substrates, (Figure 4 #6).

12. Referring to claim 35, a semiconductor wafer product, wherein the external electrodes, (Figure 4 #7 & 8C), are formed in peripheral regions of the center areas of the wiring substrates, (Figure 4 #6).

13. Referring to claim 36, a semiconductor wafer product, wherein the external electrodes are ball electrodes, (Figure 4 #7).

Allowable Subject Matter

14. Claims 21, 22, 25, 26, 32, and 33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

VAMJ
1/9/05